second control signal;

an arithmetic operation unit, connected to said comparator, accumulating an offset change amount and outputting an addition result based on said comparison result, wherein said addition result is initialized to a predetermined initial value; and

an offset voltage generator, connected to said arithmetic operation unit, generating an offset cancel voltage to cancel said offset voltage in accordance with said addition result and supplying said offset cancel voltage to said A/D converter, wherein the gain control amplifier switches the normal first amplification factor to the second amplification factor in response to said second control signal when said comparator determines that the digital signal is within the predetermined offset value range.

REMARKS

Reconsideration and allowance of the above-referenced application are respectfully requested.

I. STATUS OF THE CLAIMS

Claims 29-33, 35, 52, 56 and 60 are canceled herein.

Claims 25-28, 34 and 63-65 are amended herein.

New claims 66-71 are added.

In view of the above, it is respectfully submitted that claims 25-28, 34, 51, 53-55, 57-59 and 61-71 are currently pending and under consideration.

II. REJECTION OF CLAIMS 29, 30 AND 35 UNDER 35 U.S.C. § 102(E) AS BEING ANTICIPATED BY ZIPEROVICH (USP# 5,459,679)

Claims 29, 30 and 35 canceled herein.

In view of the above, it is respectfully submitted that the rejection is overcome.

III. REJECTION OF CLAIMS 25, 26, 33, 34, 51-58 AND 63-65 UNDER 35 U.S.C. § 103(A) AS BEING UNPATENTABLE OVER GUSMANO ET AL. (USP# 5,519,441) IN VIEW OF KOMMRUSCH (USP# 5,552,783)

Claims 33, 52 and 56 are canceled herein.

Claims 25, 26, 34 and 63-65 are amended herein. Support for the amendment to these claims may be found at page 85, lines 27-30 of the present application.

It is respectfully submitted that Gusmano and Kommrusch, either alone or in combination, do not teach or suggest an arithmetic operation unit that calculates an offset change amount based on a comparison result, which indicates whether a digital signal is within a predetermined offset value range, and an offset unit change.

Claim 25 as amended herein relates to a circuit that comprises "a comparator receiving said digital signal and determining whether said digital signal is within a predetermined offset value range, which defines allowable offset values, to output a first comparison result and a second comparison result" and "a first arithmetic operation unit connected to said comparator, calculating an offset change amount based on said first comparison result and an offset unit change," which distinguishes over the teachings of Gusmano and Kommrusch.

Independent claim 26 recite features similar to those recited in claim 25. Therefore, claim 26 also distinguishes over the teachings of Gusmano and Kummrusch.

Claims 51, 53 and 54, and claims 55, 57 and 58 depend from claims 25 and 26, respectively. Therefore, for at least the reasons that claims 25 and 26 distinguish over the cited prior art, it is respectfully submitted that claims 51, 53, 54, 55, 57 and 58 also distinguish over the cited prior art.

Claim 34 recites a method comprising "determining whether said digital signal is within a predetermined offset value range, which defines allowable offset values, to generate a comparison result" and "calculating an offset change amount based on said comparison result and an offset unit change."

Gusmano and Kummrusch, either alone or in combination, do not teach or suggest the features recited in claim 34 of the present application.

Claim 63 recites a method comprising "determining whether said digital signal is within a predetermined offset value range, which defines allowable offset values, to generate a comparison result" and "calculating an offset change amount based on said comparison result and an offset unit change."

Claim 64 recites a circuit comprising "a comparator receiving said digital signal and comparing a digital value of said digital signal with a predetermined offset value to generate a first comparison result and a second comparison result" and "a first arithmetic operation unit, connected to said comparator, calculating an offset change amount based on said first comparison result and an offset unit change."

Claim 65 recites a circuit comprising "a comparator to receive said digital signal and compare a digital value of said digital signal with a predetermined offset value to generate a comparison result" and "a first arithmetic operation unit, connected to said comparator, calculating an offset change amount based on said comparison result and an offset unit change."

Gusmano and Kummrusch, either alone or in combination, do not teach or suggest the features recited in claims 63-65 of the present application.

In view of the above, it is respectfully submitted that the rejection is overcome.

IV. REJECTION OF CLAIMS 27 AND 59-62 UNDER 35 U.S.C. § 103(A) AS BEING UNPATENTABLE OVER GUSMANO ET AL. IN VIEW OF KOMMRUSCH AND SATOH ET AL. (USP# 5,818,655)

Claim 60 is canceled herein.

Similar to the comments mentioned in section III, above, it is respectfully submitted Gusmano, Kommrusch, and Satoh, either alone or in combination, do not teach or suggest an arithmetic operation unit that calculates an offset change amount based on a comparison result, which indicates whether a digital signal is within a predetermined offset value range, and an offset unit change.

Claim 27 as amended herein, relates to a offset cancel circuit which includes "a comparator connected to said comparator, receiving said digital signal and determining whether said digital signal is within a predetermined offset value range, which defines allowable offset values, to output a first comparison result and a second comparison result" and "a first arithmetic operation unit, connected to said comparator, calculating an offset change amount based on said first comparison result and an offset unit change," which distinguishes over the teachings of Gusmano, Kommrusch, and Satoh.

Claims 59, 61 and 62 depend from claim 27. Therefore, for at least the reasons that claim 27 distinguishes over the cited prior art, it is respectfully submitted that claims 59, 61 and 62 also distinguish over the cited prior art.

In view of the above, it is respectfully submitted that the rejection is overcome.

V. REJECTION OF CLAIMS 31 AND 32 UNDER 35 U.S.C. § 103(A) AS BEING UNPATENTABLE OVER ZIPEROVICH IN VIEW OF SATOH ET AL. (USP # 5,818,655)

Claims 31 and 32 are canceled herein.

In view of the above, it is respectfully submitted that the rejection is overcome.

VI. NEW CLAIMS

New claims 66-71 are added. Support for these claims may be found at page 84, lines 25-29, page 91, lines 19-26, and page 93, lines 5-6 of the present application.

Claim 66 depends from independent claim 25. Therefore, for at least the reasons that claim 25 distinguishes over the cited prior art, it is respectfully submitted that claim 66 distinguishes over the cited prior art.

Claim 67 recites a circuit comprising "a comparator receiving said digital signal and determining whether said digital signal is within a predetermined offset value range, which defines allowable offset values, to output a comparison result," "a control circuit, connected to said comparator, generating a first control signal and a second control signal," "an arithmetic operation unit, connected to said control circuit, accumulating an offset change amount and outputting an addition result based on said first control signal," and "an offset voltage generator, connected to said arithmetic operation unit, generating an offset cancel voltage to cancel said offset voltage in accordance with said addition result and supplying said offset cancel voltage to said A/D converter, wherein the gain control amplifier switches the normal first amplification factor to the second amplification factor in response to said second control signal when said comparator determines that the digital signal is within the predetermined offset value range."

Claim 68 recites that the "second amplification factor is greater than said normal first amplification factor," and claim 69 recites that the circuit further comprises "a multiplier, connected to said comparator, calculating an offset change amount based on the comparison result and an offset unit change."

Claim 70 recites a method comprising "determining whether said digital signal is within a predetermined offset value range, which defines allowable offset values, to determine an offset change amount," "accumulating said offset change amount," "generating an offset cancel voltage for canceling said offset voltage in accordance with said accumulated offset change amount," and "switching the normal first amplification factor to the second amplification factor when the digital signal is within the predetermined offset value range."

Claim 71 recites a circuit comprising "a comparator receiving said digital signal and comparing a digital value of said digital signal with a predetermined offset value to generate a comparison result," "a control circuit, connected to said comparator, generating a first control

signal and a second control signal," "an arithmetic operation unit, connected to said comparator, accumulating an offset change amount and outputting an addition result based on said comparison result, wherein said addition result is initialized to a predetermined initial value," and "an offset voltage generator, connected to said arithmetic operation unit, generating an offset cancel voltage to cancel said offset voltage in accordance with said addition result and supplying said offset cancel voltage to said A/D converter, wherein the gain control amplifier switches the normal first amplification factor to the second amplification factor in response to said second control signal when said comparator determines that the digital signal is within the predetermined offset value range."

None of the cited prior art teaches or suggests, either alone or in combination, the features recited in claims 66-71 of the present application.

In view of the above, it is respectfully submitted that claim 66-71 patentably distinguish over the cited prior art.

VII. CONCLUSION

In view of the foregoing amendments and remarks, it is respectfully submitted that each of the claims patentably distinguishes over the prior art, and therefore defines allowable subject matter. A prompt and favorable reconsideration of the rejection along with an indication of allowability of all pending claims are therefore respectfully requested.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

STAAS & HALSEY LLP

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CERTIFICATE UNDER 37 CFR 1.8(a)

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on 20 May 2003

STAAS & HALSEY LLP

By: Mishal Valencia

Date: 5/20/03

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Please CANCEL claims 29-33, 35, 52, 56 and 60 without prejudice or disclaimer.

Please AMEND the claims in accordance with the following.

25. (TWICE AMENDED) A circuit suitable for canceling an offset voltage of an A/D converter that converts an analog signal to a digital signal, said circuit comprising:

a comparator receiving said digital signal and determining whether said digital signal is within a predetermined offset value range, which defines allowable offset values, to output a first comparison result and a second comparison result;

a first arithmetic operation unit connected to said comparator, calculating an offset change amount based on said first comparison result and an offset unit change;

[an]a second arithmetic operation unit, connected to said comparator, accumulating [an]said offset change amount and outputting an addition result based on said second comparison result; and

an offset voltage generator, connected to said second arithmetic operation unit, generating an offset cancel voltage in order to cancel said offset voltage in accordance with said addition result and supplying said offset cancel voltage to said A/D converter.

26. (TWICE AMENDED) A signal processor for receiving data information as an analog signal and processing said analog signal, comprising:

an A/D converter converting said analog signal to a digital signal; and

an offset cancel circuit, connected to said A/D converter, supplying a voltage to cancel an offset voltage of said A/D converter, said offset cancel circuit including,

a comparator receiving said digital signal, and determining whether said digital signal is within a predetermined offset value range, which defines allowable offset values, to output a first comparison result and a second comparison result;

a first arithmetic operation unit, connected to said comparator, calculating an offset change based on said first comparison result and an offset unit change;

[an] a second arithmetic operation unit, connected to said comparator, accumulating [an] said offset change amount and outputting an addition result based on said second comparison result; and

an offset voltage generator, connected to said second arithmetic operation unit, generating an offset cancel voltage in order to cancel said offset voltage in accordance with said addition result and supplying said offset cancel voltage to said A/D converter.

27. (TWICE AMENDED) A signal processor for processing a data information signal and a servo information signal, both read from a recording medium, said signal processor comprising:

a servo information processing circuit processing servo information; and

a data information processing circuit, connected to said servo information processing circuit, receiving data information as an analog signal and processing said analog signal, said data information processing circuit includes,

A) an A/D converter receiving said analog signal from an input terminal and converting said analog signal to a digital signal, to output said digital signal from an output terminal;

B) a switch connected to said input terminal of said A/D converter; and

C) an offset cancel circuit, connected between said input terminal and an output terminal of said A/D converter, supplying a voltage to cancel an offset voltage of said A/D converter, said offset cancel circuit includes,

C1) a control circuit, connected to said switch, setting said switch off to inhibit supply of said analog signal to said A/D converter when said servo information processing circuit is performing a servo information process,

C2) a comparator connected to said comparator, receiving said digital signal and determining whether said digital signal is within a predetermined offset value range, which defines allowable offset values, to output a first comparison result and a second comparison result,

C3) a first arithmetic operation unit, connected to said comparator, calculating an offset change amount based on said first comparison result and an offset unit change,

[C3)] C4) [an] a second arithmetic operation unit, connected to said comparator, accumulating [an] said offset change amount and outputting an addition result based on said second comparison result, and

[C4)] C5 an offset voltage generator connected to said second arithmetic operation unit, generating an offset cancel voltage for canceling said offset voltage in

accordance with said addition result and supplying said offset cancel voltage to said A/D converter.

28. (TWICE AMENDED) The signal processor according to claim 27, further comprising:

D) an amplifier, connected to said input terminal of said A/D converter and said control circuit, amplifying said analog signal and said offset cancel voltage by a first amplification factor, wherein said amplifier amplifies said offset cancel voltage by a second amplification factor which is higher than said first amplification factor,

wherein said second arithmetic operation unit has a reduced offset change amount inversely proportional to an increase ratio of said first amplification factor to said second amplification factor, and wherein said control circuit is connected to said comparator and said second arithmetic operation unit, and

wherein when said digital value lies within said predetermined offset value range, said control circuit controls said amplifier in such a way as to amplify said offset cancel voltage by said second amplification factor and controls said second arithmetic operation unit to perform addition based on said reduced offset change amount.

29. (CANCELED)

30. (CANCELED)

31. (CANCELED)

32. (CANCELED)

33. (CANCELED)

34. (TWICE AMENDED) A method of canceling an offset voltage of an A/D converter for converting an analog signal to a digital signal, said method comprising:

determining whether said digital signal is within a predetermined offset value range, which defines allowable offset values, to [determine an offset change amount]generate a comparison result;

calculating an offset change amount based on said comparison result and an offset unit change;

accumulating said offset change amount;

stopping said accumulating, to determine an accumulated offset change amount, when said digital value lies within said predetermined offset allowance value; and

generating an offset cancel voltage for canceling said offset voltage in accordance with said accumulated offset change amount.

35. (CANCELED)

51. (AS UNAMENDED) The circuit according to claim 25, wherein the arithmetic operation unit accumulates the offset change amount when said digital signal is not within said predetermined offset value range.

52. (CANCELED)

53. (AS UNAMENDED) The circuit according to claim 25, wherein the arithmetic operation unit supplies one of the addition result and an initial value to said offset voltage generator.

54. (AS UNAMENDED) The circuit according to claim 25, wherein the arithmetic operation unit supplies an initial value to said offset voltage generator when an offset cancel mode is initiated.

55. (AS UNAMENDED) The signal processor according to claim 26, wherein the arithmetic operation unit accumulates the offset change amount when said digital signal is not within said predetermined offset value range.

56. (CANCELED)

57. (AS UNAMENDED) The signal processor according to claim 26, wherein the arithmetic operation unit supplies one of the addition result and an initial value to said offset voltage generator.

58. (AS UNAMENDED) The signal processor according to claim 26, wherein the arithmetic operation unit supplies an initial value to said offset voltage generator when an offset cancel mode is initiated.

59. (AS UNAMENDED) The signal processor according to claim 27, wherein the arithmetic operation unit accumulates the offset change amount when said digital signal is not within said predetermined offset value range.

60. (CANCELED)

61. (AS UNAMENDED) The signal processor according to claim 27, wherein the arithmetic operation unit supplies one of the addition result and an initial value to said offset voltage generator.

62. (AS UNAMENDED) The signal processor according to claim 27, wherein the arithmetic operation unit supplies an initial value to said offset voltage generator when an offset cancel mode is initiated.

63. (ONCE AMENDED) A method of canceling an offset voltage of an A/D converter for converting an analog signal to a digital signal, said method comprising:

determining whether said digital signal is within a predetermined offset value range, which defines allowable offset values, to [determine an offset change amount]<u>generate a comparison result</u>;

<u>calculating an offset change amount based on said comparison result and an offset unit change;</u>

accumulating said offset change amount; and

generating an offset cancel voltage for canceling said offset voltage in accordance with said accumulated offset change amount.

64. (ONCE AMENDED) A circuit suitable for canceling an offset voltage of an A/D converter that converts an analog signal to a digital signal, said circuit comprising:

a comparator receiving said digital signal and [for] comparing a digital value of said

digital signal with a predetermined offset value to generate a first comparison result and a second comparison result;

a first arithmetic operation unit, connected to said comparator, calculating an offset change amount based on said first comparison result and an offset unit change;

[an]a second arithmetic operation unit, connected to said comparator, accumulating [an]said offset change amount and outputting an addition result based on said second comparison result, wherein said addition result is initialized to a predetermined initial value; and

an offset voltage generator, connected to said second arithmetic operation unit, generating an offset cancel voltage in order to cancel said offset voltage in accordance with said addition result and supplying said offset cancel voltage to said A/D converter.

65. (ONCE AMENDED) A circuit suitable for canceling an offset voltage of an A/D converter that converts an analog signal to a digital signal, said circuit comprising:

a comparator to receive said digital signal and compare a digital value of said digital signal with a predetermined offset value to generate a comparison result;

a first arithmetic operation unit, connected to said comparator, calculating an offset change amount based on said comparison result and an offset unit change;

[an] a second arithmetic operation unit, connected to said comparator, to calculate a value of the changed amount of offset between the digital value and predetermined offset value, and output a result; and

an offset voltage generator, connected to said second arithmetic operation unit, to generate an offset cancel voltage to cancel said offset voltage in accordance with the result, and supply said offset cancel voltage to said A/D converter.

Please ADD the following NEW claims:

66. (NEW) The circuit according to claim 25, wherein said first arithmetic operation unit multiplies said offset unit change by the first comparison result.

67. (NEW) A circuit suitable for canceling an offset voltage of an A/D converter that converts an analog signal to a digital signal, wherein the A/D converter is connected to a gain control amplifier that amplifies the analog signal with a normal first amplification factor or a second amplification factor, said circuit comprising:

a comparator receiving said digital signal and determining whether said digital signal is within a predetermined offset value range, which defines allowable offset values, to output a comparison result;

a control circuit, connected to said comparator, generating a first control signal and a second control signal;

an arithmetic operation unit, connected to said control circuit, accumulating an offset change amount and outputting an addition result based on said first control signal; and

an offset voltage generator, connected to said arithmetic operation unit, generating an offset cancel voltage to cancel said offset voltage in accordance with said addition result and supplying said offset cancel voltage to said A/D converter, wherein the gain control amplifier switches the normal first amplification factor to the second amplification factor in response to said second control signal when said comparator determines that the digital signal is within the predetermined offset value range.

68. (NEW) The circuit according to claim 67, wherein said second amplification factor is greater than said normal first amplification factor.

69. (NEW) The circuit according to claim 67, further comprising a multiplier, connected to said comparator, calculating an offset change amount based on the comparison result and an offset unit change.

70. (NEW) A method of canceling an offset voltage of an A/D converter for converting an analog signal to a digital signal, wherein the A/D converter is connected to a gain control amplifier that amplifies the analog signal with a normal first amplification factor or a second amplification factor, said method comprising:

determining whether said digital signal is within a predetermined offset value range, which defines allowable offset values, to determine an offset change amount;

accumulating said offset change amount;

generating an offset cancel voltage for canceling said offset voltage in accordance with said accumulated offset change amount; and

switching the normal first amplification factor to the second amplification factor when the digital signal is within the predetermined offset value range.

71. (NEW) A circuit suitable for canceling an offset voltage of the A/D converter that converts an analog signal to a digital signal wherein the A/D converter is connected to a gain control amplifier that amplifies the analog signal with a normal first amplification factor or a second amplification factor, said circuit comprising:

a comparator receiving said digital signal and comparing a digital value of said digital signal with a predetermined offset value to generate a comparison result;

a control circuit, connected to said comparator, generating a first control signal and a second control signal;

an arithmetic operation unit, connected to said comparator, accumulating an offset change amount and outputting an addition result based on said comparison result, wherein said addition result is initialized to a predetermined initial value; and

an offset voltage generator, connected to said arithmetic operation unit, generating an offset cancel voltage to cancel said offset voltage in accordance with said addition result and supplying said offset cancel voltage to said A/D converter, wherein the gain control amplifier switches the normal first amplification factor to the second amplification factor in response to said second control signal when said comparator determines that the digital signal is within the predetermined offset value range.